REMARKS

Claims 1-30 remain pending in the application.

Claims 1-30 stand rejected under 35 U.S.C. § 102(e) as being anticipated by You et al. (U.S.P. 6,799,308).

Referring to the rejection of Claims 1, 26 and 30, the Office Action states in item 3, page 2, that You et al. teach "b) identifying at least one global parameter which the delays of said early and late paths depend on".

Applicants respectfully traverse the above rejection for the following reasons:

1. You et al. state in col. 7, lines 19-21:

"In order to represent variations in clock skew from variations in clock skew from a variety of different sources, the present invention uses a **clock skew** matrix as illustrated in FIG. 5A".

Furthermore, on col. 3, lines 11-15, You et al. state:

"The method [of You's et al, sic.] **models skew** by taking into account **both systematic variations in clock arrival time and 'jitter'**, which includes the temporal variation in clock arrival time due to variables such as process, temperature, and voltage fluctuations".

Applicants submit that neither the skew nor the jitter are specifically taught in their invention, since they are not".. a global parameter which the delays of the early **AND** late paths depend on", and skew and jitter are not parameters upon which the delay of the early and late paths depend on.

2. You et al. teach a method for measuring skew while minimizing path tracing by dividing an integrated circuit into disjoint domains **a priori** and then computing "skew" relative to each domain in a separate "timing run."

In contradistinction, the method taught in the present invention selects a specific early and late mode pair of paths arriving at a particular test (which may involve elements much more general than simply latches and flip-flops), **without the need to divide the digital integrated circuit into "domains" a priori** (such a priori computation would be computationally unfeasible when considering global process variability that produces thousands or more of different possible process combinations, impacting each of the possibly millions of registers in a modern integrated circuit in a different manner). Applicants submit that You et al. require, as recited in their Claim 1;

"selecting a domain from a plurality of domains representing an integrated circuit, wherein each domain has a respective clock delay, and adding the respective skew delay relative to the selective domain"

Applicants teach away from You et al. by performing a timing analysis on the entire design of the integrated circuit or IC chip, without requiring partitioning the design into domains.

3. Still referring to item 3 of the Office Action, and more specifically, to the reading of step b) of You's et al. Claim 1, "identifying at least one global parameter which the delays of said early and late paths depend on (see fig 4a, 4b, col 4 lines 48 to col 6 line 55),

Applicants submit that the referenced portion of You et. al, describes timing verification by determining if sufficient margin (slack) exists at every timing constraint (e.g., setup or hold test) in a digital integrated circuit. You et. al, however, make no mention of identifying specific sources of variability (among all the possible sources of variability which could impact delays throughout the integrated circuit) which impact the timing of a specific test. The identification of specific sources of variability is a key concept in the method taught by Applicants in the present invention as this enables efficient coverage of the process space without resorting to full-exponential analysis for every known global source of variability.

4. Still referring to the Office Action, item 3, and with reference to step c) determining for at least one of said global parameters at least one consistent value assignment (see fig 6-10; col 8, lines 48 to col 13, lines 54, specially col 13, lines 22-30)

In the referenced portion of You et. al. "another embodiment" describes a method to "analyze parameters unique to a specific integrated chip". You et al. do not teach nor suggest setting parameters on a specific path to a consistent variable assignment. In contrast, Applicants teach in the present invention setting parameters relevant to a specific path (rather than entire chip) to a consistent variable assignment, expressly for the purpose of iterating through all such possible consistent variable assignments in order to determine the assignment which produces the worst slack for the chosen specific path.

5. Still referring to the Office Action, item 3, and with reference to step d) computing for each said consistent assignment a slack value for said path pair (see fig 6-10; col 8, lines 48 to col 13, lines 54, specially col 11, lines to col 12, lines 47).

The referenced portion of You et al. teaches a method whereby the worst slack among all possible paths between domain is recorded, however, this requires enumerating the domains a priori, which the method taught by Applicants in the present invention does not require, since such an a priori analysis would be computationally unfeasible when considering all possible combinations of process variations on all possible launching and capturing points in a digital integrated circuit.

In view of the foregoing, Applicants believe that You et al. do not anticipate Claims 1, 26 and 30, and respectfully request the rejection of the above claims based on 35 U.S.C. 102(e) be reconsidered and withdrawn.

With regard to the rejection of Claims 2-4, Applicants submit that are dependent on Claim 1, and since Applicants' Claim 1 is not believed to be anticipated by You et al., the same will also apply to all the claims dependent of Claim 1.

Notwithstanding the dependency of Claim 5 on Claim 1, in reference to the Office Action stating that You et al. teach that the initial static timing analysis is performed using bounding parameter values (see fig 6-10; col 8, lines 48 to col 13, lines 54, specially col 13, lines 22-30), Applicants submit that the method taught by You et al. describes an initial analysis using worst-case skew values. However, such a worst-case skew is only applied to the clock distribution network. In contrast, the method taught by Applicants in the present invention utilizes a bounded parameter value assignment for the entire digital integrated circuit such that all delays for late paths are computed assuming slowest possible conditions (with respect to the sources of variability under consideration) and all delays for early paths are computed assuming fastest possible conditions for said sources of variability. Furthermore, by using a bounded parameter value assignment rather than a global worst case skew, tests which involve longer delay paths are naturally penalized more than tests involving shorter delay paths which produces less pessimistic initial timing as compared to using a single "worst case skew" which would need to penalize all tests by the worst possible skew attainable for any single test.

Similarly, with respect to Claim 6, the Office Action states that You. et al. teach " further comprising the step of determining for each of said timing tests the worst of said timing tests the worst of said computed slacks" (see fig 4a-4b col 5 lines 39 to lines 41 and summary).

The method taught by You et al. involves recording to the top failing paths terminating in each domain separately, whereas the method taught by Applicants in the present invention records the worst slack for a particular path terminating at a particular test across all possible legal process assignments.

With regard to Claims 7 and 27, the Office Action states that You et al. teach that " step c) further comprises the steps of e) enumerating combinations of realizable values of at least one of said identified parameters (see fig 6-10; col 8, lines 48 to col 13, lines 54 especially col 13, lines 22-30)" and "step f) performing a timing analysis for each of said enumerated combinations (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13 lines 22-30)",

Applicants submit that You et. al describes "analyzing" parameters specific to an "integrated circuit chip plan" does not teach nor suggest the method taught by Applicants which specifically prescribes identifying global sources of variability affecting a particular path, and setting at least one of said parameter to a physically realizable value

(Note in particular that the method taught by Applicants in the present invention does not require dividing the integrated circuit in to separate domains a priori.

Regarding Claim 8, the Office Action states that You et al. teach that "step e) is terminated after one of the timing analyses of step step e) produces a slack below a specified threshold (see fig 6-10 ; col 8, lines 48 to col 13, lines 54, especially col 13, lines 22-30)".

Applicants submit that the method taught by You et al. requires collecting the "top N paths" terminating in a particular domain, whereas the method taught in the present invention terminates the analysis of a specific path once the slack for a given parameter combination falls below a specified threshold (Note that the method taught in You et. al does not envision a slack threshold to limit analysis of a particular path).

Regarding Claim 9, the Office Action states that You et al. teach "at least one parameter whose realizable values are enumerated comprises a subset of the parameters identified in step b) (see fig 4a-4b; col 4, lines 48 to col 6, line 55)",

Applicants submit that You et. al, make no mention of and do not teach nor suggest identifying specific sources of variability (among all the possible sources of variability which could impact delays throughout the integrated circuit) which impact the timing of a specific test. The identification of specific sources of variability is a key concept in the method taught in the present invention since it enables efficient coverage of the process space without resorting to full-exponential analysis , e.g., as would be required for a priori identification of domains.

Accordingly, Applicants believe that Claim 1-30 are not anticipated by You, and respectfully request that the rejection of Claim 1-30 based on 35 U.S.C. §102(e) be reconsidered and withdrawn.

In view of the foregoing, it is respectfully requested that all the outstanding rejections to this application be reconsidered and withdrawn and that the Examiner pass all pending claims to issue.

Should the Examiner have any suggestions pertinent to the allowance of this application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,
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